Modified PTO/SB/33 (10-05)

PRE-APPEAL BRIEF REQUEST FOR REVIEW	Docket Number Q53743	
Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450	Application Number 09/273,560	Filed March 22, 1999
	First Named Inventor Takumi HASEGAWA	
	Art Unit 2123	Examiner Kandasamy THANGAVELU

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23373
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Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal

The review is requested for the reasons(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

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June 22, 2009
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PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Takumi HASEGAWA

Appln. No.: 09/273,560

Confirmation No.: 7269

Filed: March 22, 1999

For: DELAY ANALYSIS SYSTEM

Docket No: Q53743

Group Art Unit: 2123

Examiner: Kandasamy THANGAVELU

PRE-APPEAL BRIEF REQUEST FOR REVIEW

MAIL STOP AF - PATENTS
Commissioner for Patents
P.O. Box 1450
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Sir:

Pursuant to the Pre-Appeal Brief Conference Pilot Program, and further to the Examiner's Final Office Action dated January 23, 2009, Appellants file this Pre-Appeal Brief Request for Review. This Request is also accompanied by the filing of a Notice of Appeal.

Claims 1-6 are all the claims pending in the application. Appellants turns now to the rejections at issue.

Claim Rejections – 35 U.S.C. § 101

Claim 3 is rejected under 35 U.S.C. § 101 because the claimed method could allegedly be construed as being implemented without a computer (Final Office Action, page 4, paragraph 5.1). In the previous Amendment filed April 23, 2009 ("previous Amendment"), claim 3 was amended to recite "A computer-implemented method…". Therefore, Appellants submitted that claim 3 complies with the requirements of 35 U.S.C. § 101.

In the Advisory Action dated May 13, 2009, it is indicated that the claim 3 amendment has not been entered. Further, the Examiner contends that the claim still does not comply with the requirements of § 101 because "though the preamble of claim 3 indicated that the method is computer implemented, none of the steps is indicated to be implemented on a computer" (Advisory action, page 2, sixth paragraph). Although Appellants do not agree with the Examiner's position on this point, Appellants amend claim 3 in the concurrently filed Amendment under 37 C.F.R. § 41.33. Under the provisions of 37 C.F.R. § 41.33, an amendment can be made after the filing of a Notice of Appeal to narrow the issues on appeal. As such, since the amendment to claim 3 places the application in better form for appeal, Appellants respectfully request entry of the amendment.

Specifically, the amendment to claim 3 recites that the delay analysis library is referenced "using a computer". Accordingly, Appellants submit that the claim complies with the requirements of § 101.

Claim Rejections – 35 U.S.C. § 112

Claims 5 and 6 stand rejected under 35 U.S.C. § 112, first paragraph as allegedly failing to comply with the written description requirement. For *at least* the following reasons, Appellants respectfully traverse the rejection.

Appellants submit that the arguments submitted in the Amendment filed October 8, 2008 ("October 8th Amendment") sufficiently pointed out portions of the Specification and drawings which support the features recited in claims 5 and 6. In response to these arguments, the Examiner confusingly, and inaccurately, asserts that the middle column of FIG. 3 ('Rise/fall') is "totally incorrect" (Final Office Action, page 15, last paragraph, and page 17, first paragraph). Specifically, the Examiner thinks that the determination that no delay ('NONE') was caused by the input, as recited in claim 6, is incorrect. Appellants respectfully disagree.

For instance, as discussed in the Specification, and as pointed out during the phone interview conducted on April 16, 2009, since the state of the output is low both at the first clock signal (when input 1 rises), and at the second clock signal (when input 2 falls), it is determined that no delay was caused by the input (Specification, page 7, line 22 to page 8, line 6, and FIG. 3). As such, contrary to the Examiner's assertions, the determination of 'NONE" in FIG. 3 is justified.

Claim 5 recites that the delay analyzing module determines automatically, based on the logical operation information of the logical circuit, that there is no change in a signal state of an output terminal of the logical circuit, and when no change in the signal state is determined, the delay analyzing module determines that no further delay analysis needs to be performed.

At least page 7, line 22 to page 8, line 6 of the Specification, and FIGS. 3-5 of the Appellants' drawings support the above-noted features of claim 5. FIG. 3 is a waveform diagram showing the rise and fall delay patterns of a 2-input AND circuit, according to a non-limiting, exemplary embodiment of the present invention. That is, FIG. 3 is an example of the claimed delay time information in the delay analysis library. In the case where the input 1 rises and the input 2 falls, the Specification discloses that "no terminal is selected for delay analysis" (Specification, page 8, lines 5 and 6). That is, when no change in a signal state of an output terminal of the logical circuit is determined (see FIG. 3, middle column – 'Rise/fall'), the delay analyzing module determines that no further delay analysis needs to be performed. Moreover, this determination is necessarily automatic since it is based on the logical operation information of the logical circuit, which is stored in the delay analysis library. Therefore, Appellants respectfully submit that claim 5 complies with the requirements of 35 U.S.C. § 112.

Appellants further submit that the features of claim 6 are supported by the Appellants' disclosure. For example, claim 6 recites that the logical circuit is an AND gate, and when the logical operation

information of the AND gate in the delay analysis library indicates that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals, and at a time at which the second clock signal among the two clock signals is input, the state is LOW which is regarded to be the same state as the first signal state, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to a clock signal, the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, based on the delay time information labeled as NONE, automatically determines that no further delay analysis needs to be performed in this case.

Appellants respectfully submit that the portions of the Specification and Appellants' drawings discussed above with respect to claim 5 also support the features of claim 6. It appears that the Examiner's position is that since the claim features at issue are allegedly not found explicitly in the Appellants' Specification, the subject claim limitations must not be supported by the Appellants' disclosure. **Appellants' respectfully submit, however, that there is no *in haec verba*—i.e., word for word—requirement for satisfying the written description requirement.** Therefore, contrary to the Examiner's assertions, Appellants are not burdened to show where the claimed terms are explicitly recited in the Specification. **Rather, the newly added claim limitations can be supported in the Specification through express, implicit, or inherent disclosure** (*Lockwood v. American Airlines, Inc.*, 107 F.3d 1565, 1572, 41 USPQ2d 1961, 1966 (Fed. Cir. 1997 as cited in MPEP § 2163.02). Additionally, Appellants can show possession of the claimed invention by describing the claimed invention with all of its limitations using such descriptive means as **words, structures, figures, diagrams, and formulas** that fully set forth the claimed invention. *Id.*

Here, in a non-limiting, exemplary embodiment of the claimed delay time information shown in FIG. 3, it is shown in the middle column of the table in FIG. 3 (the 'Rise/fall' column) that the state of the output terminal of the AND gate changes LOW-HIGH-LOW within a period of two clock signals. Further, it is shown that at a time at which the second clock signal among the two clock signals is input, the state is LOW which is the same state as the first signal state (i.e., at the first clock signal). Accordingly, the delay analysis library does not recognize a rise (LOW-HIGH) at the output terminal of the AND gate corresponding to the clock signal (see Specification, page 8, lines 5 and 6), and thus, in this case the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate. Therefore, the delay analyzing module, based on this delay time information, automatically determines that no further delay analysis needs to be performed as recited in claim 6. *Id.* As such, Appellants respectfully submit that claim 6 complies with the requirements of 35 U.S.C. § 112.

Claim Rejections – 35 U.S.C. § 103

Claims 1-4 are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,041,168 to Hasegawa ("Hasegawa '168") in view of U.S. Patent No. 5,528,511 to Hasegawa ("Hasegawa '511"). For *at least* the following reasons, Appellants respectfully traverse the rejection.

Appellants note that in the Amendment filed February 15, 2008, it was submitted that there is no delay time information in Hasegawa '511 which is **specific to** an input terminal logical **state transition** (e.g., at input terminals 's' or 'v', see FIGS. 4 and 5) and a resulting logical **state transition** at an output terminal (e.g.,, at output terminal 't'), as required by claim 1. Moreover, it was submitted that the delay times shown in FIGS. 12 and 13 of Hasegawa '511 are identified between the input terminals 's' or 'v' and the output terminal 't'. On the other hand, with the configuration set forth in claim 1, a target point at which no further delay analysis is required is automatically determined (see February 15th Amendment, page 7, last paragraph to page 8, first full paragraph).

In response, in the last Office Action dated July 9, 2009 ("last Office Action"), the Examiner contends that "**Hasegawa** '511 shows at Fig. 3 the logical state transitions at each input terminal and logical state transitions at each output terminal. **Hasegawa** '511 discusses at CL1, L28-35 the logical state transitions at the input terminal and the output terminal, using rise/fall terms. **Hasegawa** '511 states at CL2, L30-42 that the delay time of the upper route having larger delay has no effect on the determination of the delay time of the OR gate (invalid). The logical operation information is stored in the computer (library) representing correspondence between logical state transitions at each input terminal of the at least one circuit and logical state transitions at each output terminal of the at least one circuit. **Hasegawa** '511 describes at CL3, L5-26 that the delay time information is stored for each rise/fall type signal at various input and output nodes, an arc with invalid rise/fall signal is invalidated and the delay time is obtained for the logic circuit after the arcs are modified. Therefore, **Hasegawa** '511 teaches a delay time information that is specific to an input terminal logical state transition and resulting logical state transition at an output terminal, as this provides correct delay time even when either of rise or fall of the signal has no effect in a delay time computation process (CL2, L61-65)" (last Office Action, page 17, first full paragraph). In the October 8th Amendment, Appellants respectfully disagreed as follows.

Appellants submitted that the invalidness specifier indicated by the invalidness specification in FIG. 7 of Hasegawa '511 is not, and cannot be, automatically generated unlike the delay time information of claim 1. This is because in Hasegawa '511, the "OR DEVICE" of FIG. 2 is not always an OR device, and moreover, there is no information provided in Hasegawa's alleged delay analysis library of what logical circuit is the subject of the delay analysis. Specifically, Hasegawa '511's FIG. 3 is merely one example, which does not form the basis that the information of FIG. 7 is correct in all cases. Thus, **manual** judgment is necessary for preparing the information indicated by the invalidness specifier of FIG. 7. On the other hand, in the present invention as claimed, the delay analysis library already comprises logical operation information which in turn comprises the delay information of the logical circuit, based on which the delay analyzing module can automatically analyze the delay of the logical circuit (e.g., the delay analyzing module, based on the delay time information, can generate indicative information that an action is invalid or valid). Hasegawa '511, alone, or in combination with Hasegawa '168, does not teach or suggest this feature.

The Examiner's response in the Final Office Action to the above-noted previously submitted arguments from the October 8th Amendment is basically the same as the last Office Action (e.g., see Final Office Action, page 18, last paragraph, and last Office Action, page 17, first full paragraph). The only difference in the Final Office Action is lines 2-7 on page 19, but here, the Examiner again points to previously cited portions of the references which allegedly teach that manual judgment is not necessary in Hasegawa '511 for preparing the information indicated by the invalidness specifier of FIG. 7. Appellants respectfully disagree.

For example, in the Examiner's response on page 19 of the Final Office Action, it is alleged that Hasegawa '168, in col. 1, lines 58-61 and col. 2, lines 30-35 teaches a library that already contains logical operation information. Appellants submit, however, that this logical operation does not teach or suggest all the features of the claimed logical operation information. For example, the claimed logical operation information comprises delay time information which is **specific to** an input terminal logical **state transition** and a resulting logical **state transition** at an output terminal. Although Hasegawa '168 discloses storing a delay time from each pin of a starting point in the logical circuit to a pin corresponding to the ending point, it does not teach or suggest that the stored delay time is specific to a state transition of the pin. Moreover, neither Hasegawa '511 nor Hasegawa '168 teach that the type of logic circuit which is the subject of delay analysis is prestored. As such, the delay analysis cannot be automatic, as required by claim 1. Consequently, Hasegawa '511 alone, or in combination with Hasegawa '168, does not render claim 1 obvious.

Claims 2-4 recite features similar to those discussed above with respect to claim 1. Therefore, claims 2-4 are patentable for *at least* reasons similar to those given above with respect to claim 1.

Conclusion

In view of the foregoing, Appellants respectfully request withdrawal of the improper 35 U.S.C. § 101, 35 U.S.C. § 112, and 35 U.S.C. § 103 rejections.

The USPTO is directed and authorized to charge any required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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Date: June 22, 2009